

REMARKS

In the March 21, 2004 Office Action, the Examiner:

- Rejected claims 112, 112 and 116-122 under 35 U.S.C. 103(a) as unpatentable over Bellomo et al. ("*Bellomo*", U.S. Pat. No. 5,419,712) in view of Estes ("*Estes*", U.S. Pat. No. 5,214,563).

Applicants retain the claims in their current form and respectfully present arguments for their allowance.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 112, 113 and 116-122 under 35 U.S.C. 103(a) as unpatentable over *Bellomo* in view of *Estes*. This set of claims contain one independent claim, namely independent claim 112. In rejecting claims under 35 U.S.C. § 103(a), the patent Examiner bears the initial burden of supporting all three elements of a *prima facie* case of obviousness.¹ First, the prior art references must, when combined, teach or suggest all claim limitations.² Second, the Examiner must identify a suggestion in the prior art references or other motivation to combine their teachings.³ Finally, there must be a reasonable expectation of success.⁴ "If the Examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned."⁵

A. The Cited Documents Do Not Teach All The Claim Limitations

As will be shown below, the combination of Bellomo and Estes does not teach at least three of the limitations of independent claim 112, including (i) a chip package, (ii) compliant

¹ See MPEP § 2142.

² See *id.* § 2143.03.

³ See MPEP § 2143.01.

⁴ See *id.* § 2143.02.

⁵ See *In re Rijckaert*, 9 F.3d 1531, 1532 (Fed. Cir. 1993) (internal citations omitted).

contacts, and (iii) that the contacts are for detachable electrical coupling to a circuit board. Accordingly, independent claim 112 cannot be unpatentable over the combination of Bellomo and Estes, as the references do not teach or suggest all claim limitations.

The Examiner states that “Bellomo discloses a chip socket assembly comprising: a chip package (36) . . .” However, Bellomo teaches a edge card interconnection system 30 having a module 36 that includes a plurality of memory modules 38.⁶ Unlike Bellomo, the claimed “chip package” is a well known term of art that means a housing that surrounds an integrated circuit, and cannot be likened to the “module 36” taught by Bellomo.

It is well established law that claim terms carry their ordinary and customary meaning as viewed by persons of skill in the pertinent art.⁷ The claims, however, “must be read in view of the specification,”⁸ as the specification “is the single best guide to the meaning of a disputed term.”⁹ Furthermore, “[d]ictionaries or comparable sources are often useful to assist in understanding the commonly understood meaning of words.”¹⁰

Not only is the ordinary and customary meaning of a “chip package” well known to persons of skill in the art, but the present specification consistently uses the term to include the packaging or housing that directly surrounds an integrated circuit. For example, the specification refers to a number of examples of chip packages that are known in the art, including a surface vertical package (“SVP”)¹¹ and a surface horizontal package (“SHP”).¹² The present specification further states that the “chip package includes packaging material

⁶ Bellomo at col. 4, ll. 14-26.

⁷ See *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369 (Fed. Cir. 2003); *Tex. Digital Sys. v. Telegenix, Inc.*, 308 F.3d 1193, 1202 (Fed. Cir. 2002); *Boehringer Ingelheim Vetmedica, Inc. v. Schering-Plough Corp.*, 320 F.3d 1339, 1346 (Fed. Cir. 2003).

⁸ See *Markam v. Westview Instruments, Inc.*, 52 F.3d at 979.

⁹ See *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576 (Fed. Cir. 1996) at 1582.

¹⁰ See *Phillips v. AWH Corp.*, (Fed. Cir. 2005).

¹¹¹¹ Present specification at para. 0003.

that contains an integrated circuit.”¹³ Furthermore, the specification clearly distinguishes between a “chip package” and a “module.” For example, the present specification discloses “prior art modules 321, 331, 341, and 351.”¹⁴ This ordinary and customary meaning of the term “chip package” is further supported by the remainder of the claim itself, which states that “an integrated circuit disposed within the chip package, the integrated circuit electrically coupled to the plurality of compliant contacts,” i.e., the chip package houses the integrated circuit. Even further support for the term’s ordinary meaning is evidenced by the term’s dictionary definition, *i.e.*, a “housing that chips come in for plugging into (socket mount) or soldering onto (surface mount) the printed circuit board.”¹⁵ In light of the above, it is clear the meaning of a “chip package” is the packaging or housing that surrounds an integrated circuit, and as such, cannot be likened to the module 36 taught by Bellomo. Rather, the module in Bellomo includes multiple memory modules 38 electrically interconnected with a main circuit board 33.¹⁶ Accordingly, Bellomo does not disclose, teach or suggest the “chip package” claimed in independent claim 112.

Furthermore, it should be noted that independent claim 112 requires that the “chip package [has] second and third sides formed with oppositely disposed protrusions.” In other words, the chip package itself includes the protrusions. However, the features of Bellomo that the Examiner relies on for the protrusions extend from the module 36, and not from any chip package. As stated above, a module is not the “chip package” claimed in independent claim 112.

In addition, the Examiner states that “Estes discloses a chip package (110) with a plurality of compliant contacts (120) . . .” (Emphasis added). However, Estes only teaches “a

¹² Present specification at para. 0006.

¹³ Present specification at para. 0020.

¹⁴ Present specification at para. 0068.

¹⁵ See Computer Desktop Encyclopedia, Freedman, Mc Graw Hill 9th ed. 2001.

semiconductor device including a plurality of ‘J’ shaped leads 120 extending from a molded ceramic or plastic package 110.”¹⁷ Estes, however, makes no mention that the leads are “compliant.”

In the Final Office Action, the Examiner states that “it appears that the structure of the leads (i.e, cantilevered conductive leads) provide the lead with inherent flexibility.”

Furthermore, During the above mentioned telephone interview, the Examiner indicated that the “J” shaped leads 120 disclosed in Estes are inherently compliant.

Applicants respectfully submit that not only does Estes not teach compliant contacts, but the Examiner’s inherency rejection is improper. Under the law, an Examiner faces a rigorous standard in asserting that teachings not expressly disclosed in a prior art reference are nevertheless inherent:

In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art.¹⁸

As *Levy* makes clear, the allegedly inherent characteristic must necessarily flow from the teachings of the cited prior art. “The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient [to establish inherency].”¹⁹ A mere possibility or probability is simply not enough to support inherency.²⁰

¹⁶ Chip packages, generally do not include a circuit boards, and instead include the chip within packaging material.

¹⁷ Estes, col. 3, ll. 61-63.

¹⁸ See *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (italics in original; underlining added); MPEP 2112.

¹⁹ See *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing the Examiner’s inherency rejection) (citations omitted).

²⁰ See *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

Furthermore, not only must the allegedly inherent subject matter be necessarily present, it must be “recognized by persons of ordinary skill” to be necessarily present.²¹ This is particularly significant where inherency is applied in an obviousness setting because “obviousness cannot be predicated on what is not known at the time an invention is made, even if the inherency of a certain feature is later established.”²² Applying these strict standards required by the rules and case law, Applicants respectfully submit that the inherency rejections be withdrawn, as *Estes* does not teach or suggest that the “J” shaped leads are compliant.

Furthermore, the Examiner states that “*Estes* discloses . . . each compliant contact adapted to detachably electrical [couple] to a circuit board to enable a flexible and reliable mounting.” (Emphasis added). The Examiner further states that “[i]n response to Applicant’s arguments that ‘[a] soldered connection is not detachable’, please note that a soldered connection can be detached by force or heat, for example.” It is respectfully submitted that this argument is unsound. If the Examiner’s argument were true, the term “detachable” would have no meaning at all, as any permanent bond can be broken if enough heat or force is applied.

Rather, the term “detachably” or “detachable” must be given its ordinary and customary meaning to one skilled in the art. One skilled in the art certainly will not interpret a soldered connection to be a detachable connection. Therefore, not only is the ordinary meaning of the term “detachable” clear to those skilled in the art, but the specification clearly describes removing or detaching the chip package from the base without requiring excessive heat or force. For example, the specification provides “for the capability [of] users to remove

²¹ See *Metabolite Laboratories, Inc. v. Laboratory Corp. of Am. Holdings*, 370 F.3d 1354, 1367 (Fed. Cir. 2004) (quoting *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991).

²² See *In re Rijckaert*, 9 F.3d at 1534; MPEP 2141.02.

chips from a circuit board with relative ease”²³ and that “[c]hip 1840 may be removed from base 1810 by pushing left clip portion 1817 outward toward the left until protruding ledge 1833 is no longer beneath the upper lip of socket 1877 while lifting chip 1840 from base 1810.”²⁴ The ordinary meaning of the term “detachable” is also supported by the term’s dictionary definition, i.e., capable of being “separated; disconnected.”²⁵ In light of the above, it is clear that permanently soldering a lead to a circuit board, as disclosed by Estes, cannot be likened to compliant contracts for detachable electrical coupling to a circuit board, as claimed in independent claim 112 of the present invention.

For at least the reasons stated above, it is respectfully submitted that the combination of Bellomo and Estes does not disclose, teach or suggest all of the limitations of independent claim 112, and, therefore, cannot sufficiently establish a *prima facie* case of obviousness.

Accordingly, claims 112, 113 and 116-122 cannot be unpatentable over *Bellomo* in view of *Estes*, as the prior art references do not teach or suggest all of the claim limitations.

B. There is No Motivation to Combine the Cited Documents

Additionally, the obviousness rejections are improper because there is no motivation to combine Bellomo with Estes. The MPEP requires the Examiner to identify “some objective teaching in the prior art or [show] that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.”²⁶ “Combining prior art references without evidence of such a suggestion, teaching or motivation simply takes the inventor’s disclosure as a blueprint for piecing

²³ Present specification, para. 011.

²⁴ Present specification, para 0128.

²⁵ See The American Heritage College Dictionary, 378, 3rd ed. 1997.

²⁶ See *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988).

together the prior art to defeat patentability – the essence of hindsight.”²⁷ Thus, the requirement that the Examiner identify objective evidence of a suggestion or motivation to combine is a critical safeguard against “the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.”²⁸ In short, the suggestion to combine references turns on evidence, not the “PTO’s speculation.”²⁹

Further, PTO reliance on common knowledge and common sense in rejecting claims does not fulfill the PTO’s obligation to create a proper record.³⁰ Such reliance, which would support combining virtually any references, would preclude most patents:

[V]irtually all [inventions] are combinations of old elements. Therefore, an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue.³¹

Common knowledge and common sense may be applied to the evidence but are not themselves a substitute for evidence.³² For this reason, if the Examiner fails to “explain the specific understanding or principle within the knowledge of a skilled artisan that would motivate one with no knowledge of [the present] invention to make the combination,” the Federal Circuit will infer that the Examiner selected these references with the assistance of hindsight.³³

As support for the combination the Examiner merely states that “it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the chip package of Bellomo with flexible leads, as taught by Estes, to enable a flexible and

²⁷ See *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999) (abrogated on other grounds by *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000)).

²⁸ See.” *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999).

²⁹ See *In re Jones*, 958 F.2d 347, 351 (Fed. Cir. 1992).

³⁰ See *In re Thrift*, 298 F.3d 1357, 1364 (Fed. Cir. 2002).

³¹ See *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998) (internal citations omitted).

³² See *In re Lee*, 277 F.3d 1338, 1345 (Fed. Cir. 2002).

³³ See *Rouffet* at 1358 (emphasis added).

reliable mounting.” For the following reasons Applicants respectfully submit that there is no motivation for the Examiner’s suggested combination.

First, Bellomo and Estes are not in the same field of endeavor. Bellomo relates to a module edge card interconnection system, while Estes relates to a thermally reactive lead assembly. These are two very different technologies, each with its own unique set of advantages and disadvantages, and associated technical challenges. In other words, one of ordinary skill in the art would not be motivated to combine the teachings of a module edge card interconnection system with those of a thermally reactive lead assembly.

Second, the Examiner’s stated reasons for the motivation to combine are not supported by the law. The Examiner states that the combination of is proper because “it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the chip package of Bellomo with flexible leads, as taught by Estes, to enable a flexible and reliable mounting.” Applicants respectfully submits that this is not objective evidence of a motivation to combine. The Examiner merely appeals to “common sense” to support combining the cited documents for purposes of providing a flexible and reliable mounting. A proper obviousness rejection requires more. As explained above, if the Examiner fails to clearly explain the specific understanding or principle within the knowledge of one ordinary skill in the art that would motivate him to make the combination, it will be inferred that the Examiner selected the cited documents with the assistance of hindsight.

For at least the reasons discussed above, Applicants respectfully submit there is no motivation to combine Bellomo with Estes, and therefore, that the obviousness rejection be withdrawn.

C. There is No Reasonable Expectation of Success If The References Were Combined

This element of a *prima facie* case of obviousness requires the Examiner to show, without resort to hindsight, that the combination of the prior art references was based on a reasonable expectation of success.³⁴ More particularly, the Examiner must establish the existence of a reasonable expectation that a beneficial result will be achieved through the combination of the prior art references.³⁵ The determination of whether the proposed combination of the prior art references has a reasonable expectation of success is made as of the time of the invention.³⁶

It is unclear how a combination of the two references would operate, let alone provide a beneficial result. If one skilled in the art were to combine the “J” shaped leads from Estes with the teachings of Bellomo one would have a module 36 (Bellomo) that is permanently soldered to a circuit board. This combination would have no advantages over the separate teachings of the references. In fact, the soldered J-shaped leads of Estes would vitiate any utility between the edge card interconnection system 30 and the connector portion 32 taught by Bellomo. As a result, one skilled in the art would not have any reasonable expectation that combining the interconnection system of Bellomo with the “J” shaped leads of Estes would result in a successful system.

³⁴ See *In re Merck & Co., Inc.*, 800 F.2d 1091, 1098 (Fed. Cir. 1986).

³⁵ See *In re Longi*, 759 F.2d 887, 897 (Fed. Cir. 1985).

³⁶ See MPEP § 2143.02.

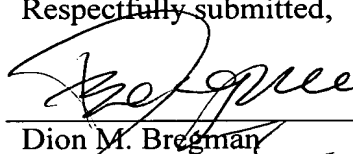
CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner has failed to establish a *prima facie* case of obviousness. Accordingly, it is respectfully submitted that the rejections contained in the Final Office Action are improper and should be withdrawn. If the Examiner believes that the present matter can be resolved without Appeal, Applicants encourage the Examiner to call the undersigned attorney at 650-843-7519 to set up an interview to deal with any remaining issues.

If there are any fees or credits due in connection with the filing of this Amendment, including any fees required for an Extension of Time under 37 C.F.R. Section 1.136, authorization is given to charge any necessary fees to our Deposit Account No. 50-0310 (order No. 60809-5054-US). A copy of this sheet is enclosed for such purpose.

Respectfully submitted,

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